



FIG. 1

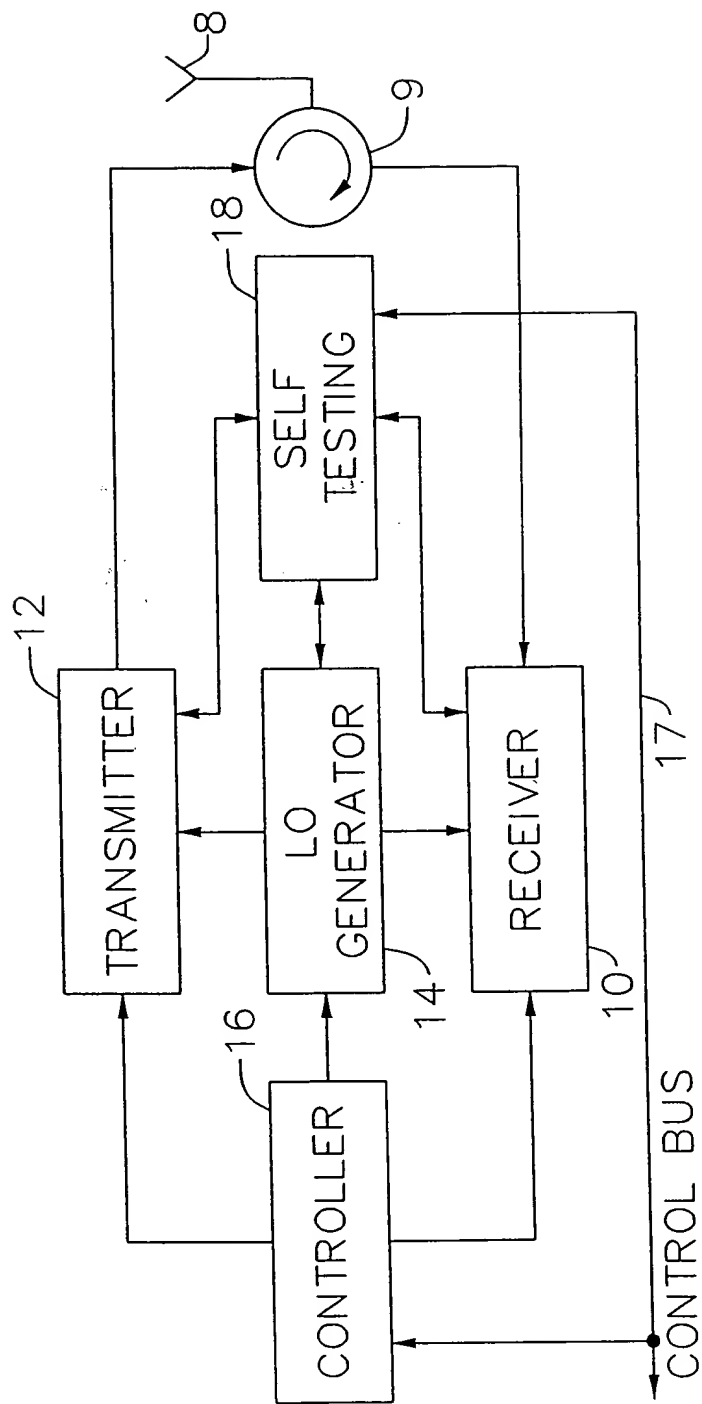


FIG. 2

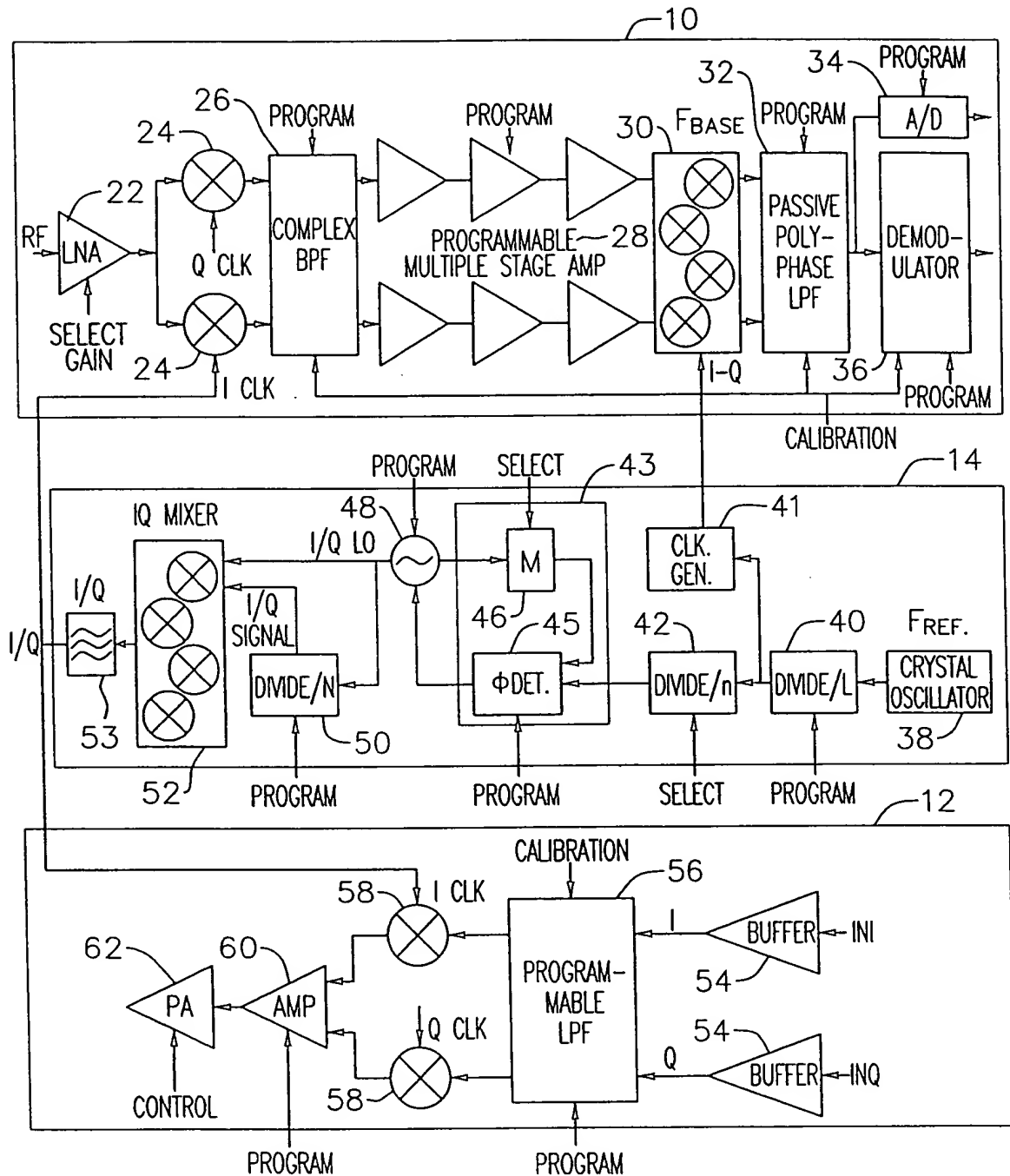


FIG. 3

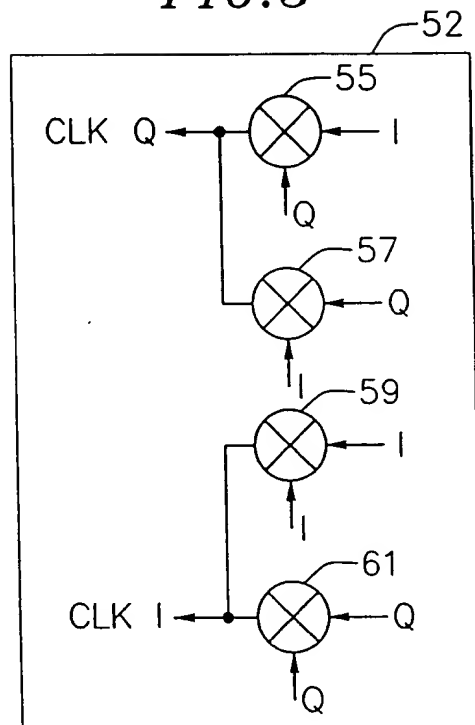


FIG. 4

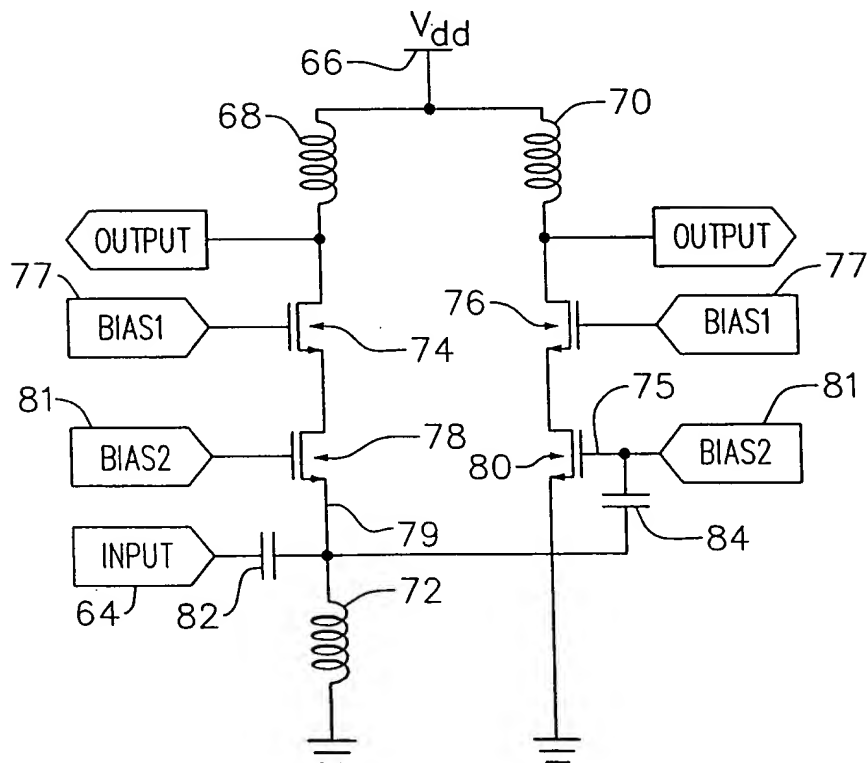


FIG. 4(a)

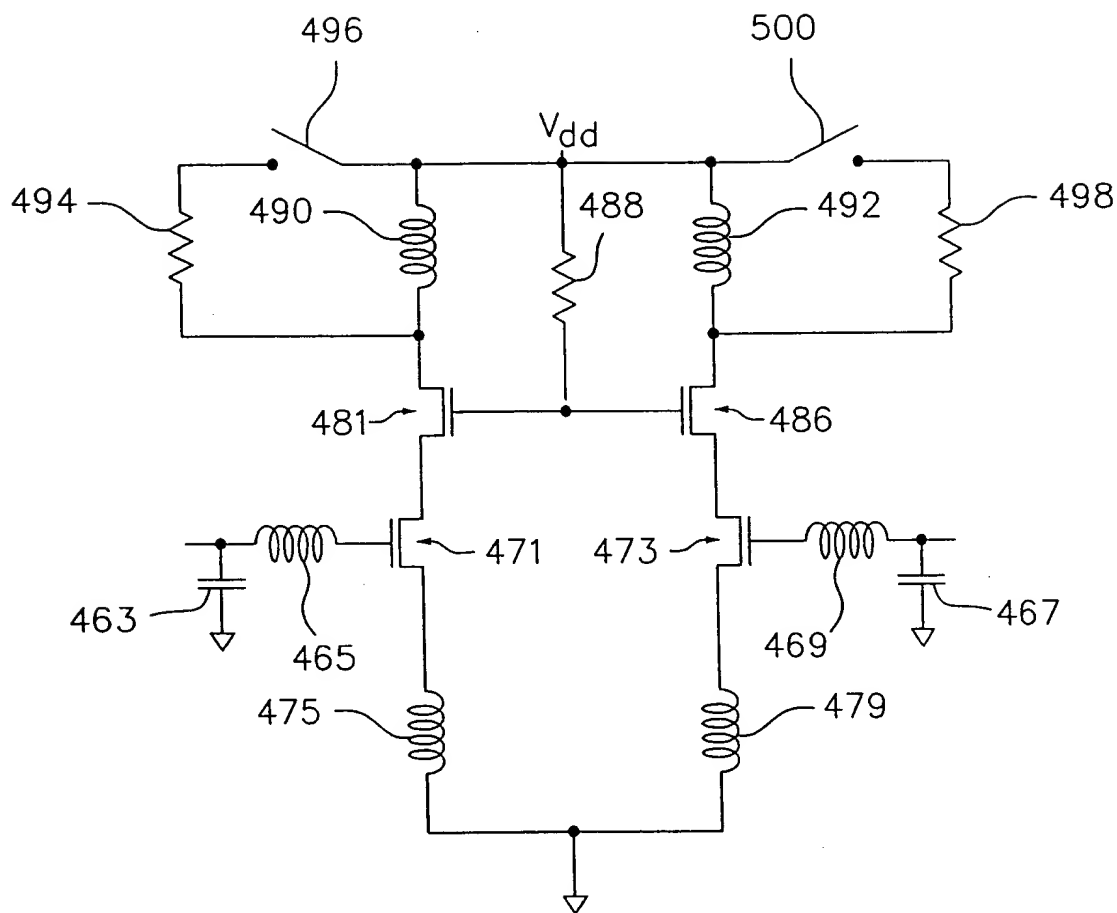


FIG. 5

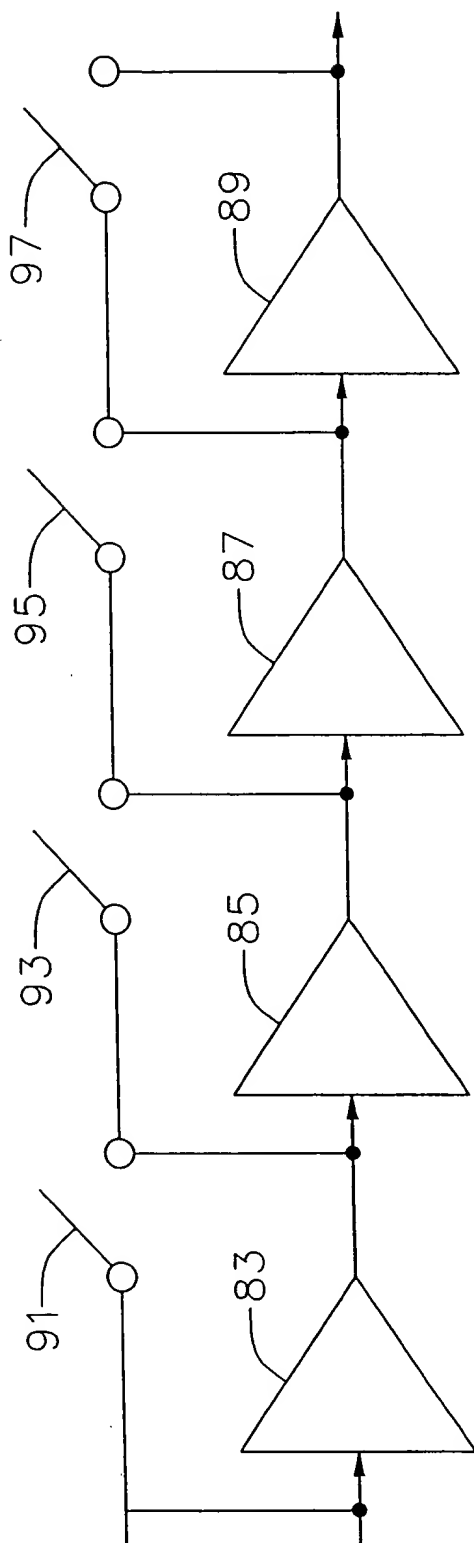


FIG. 6

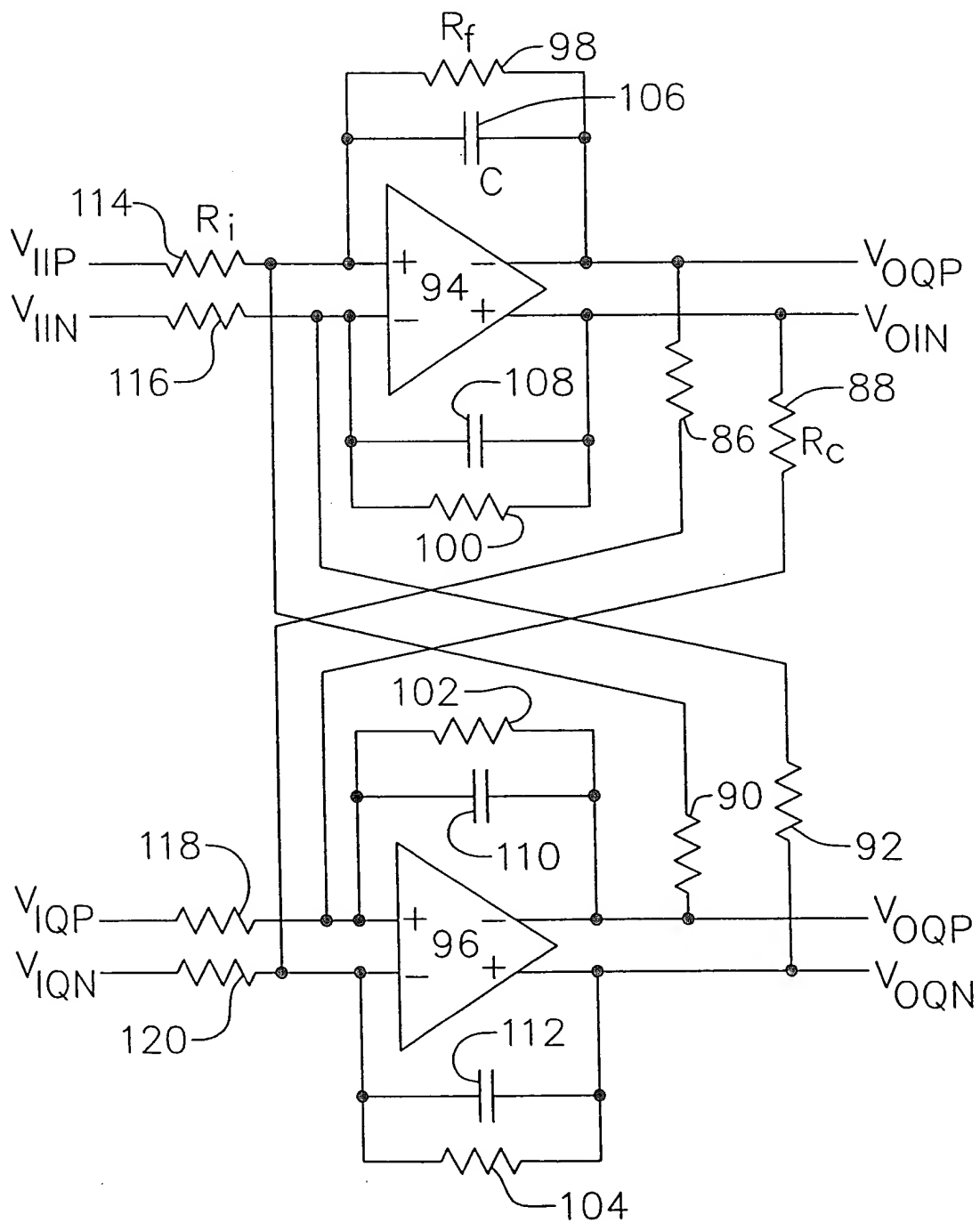


FIG. 7

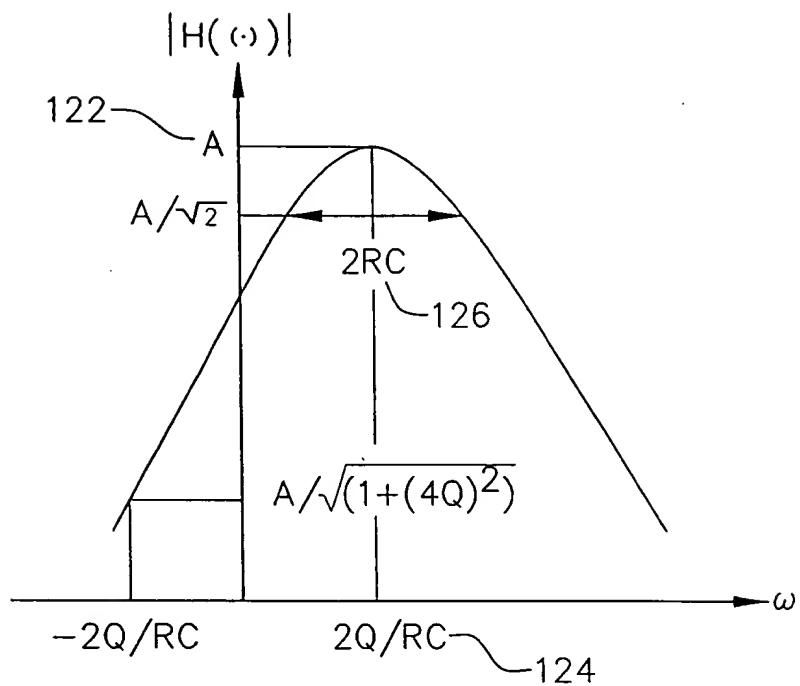


FIG. 8

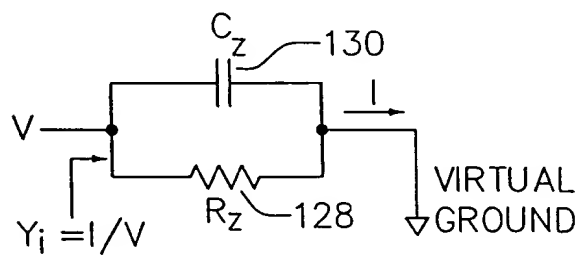


FIG. 9

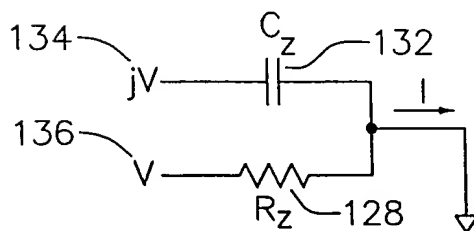


FIG. 10

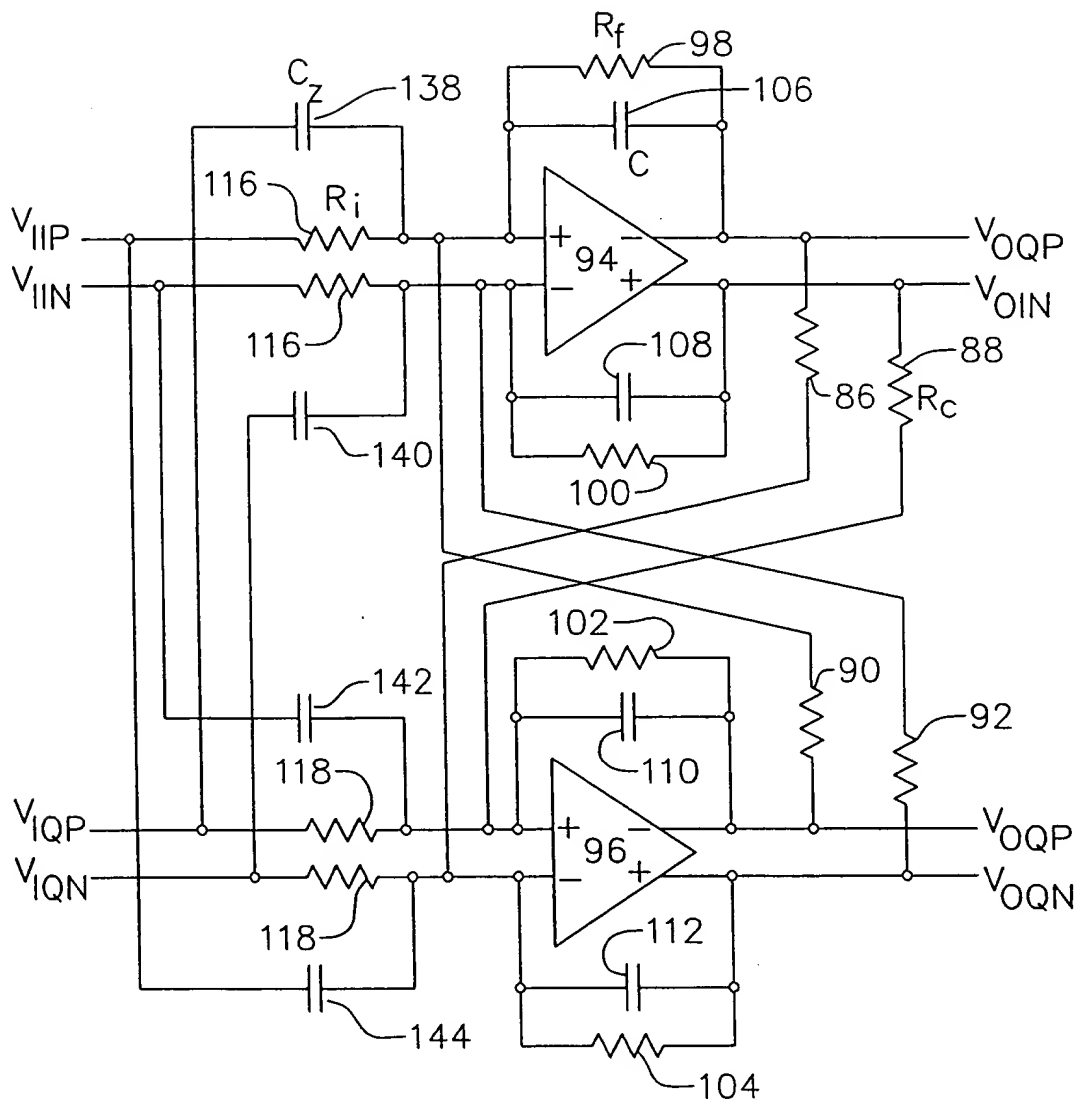




FIG. 11

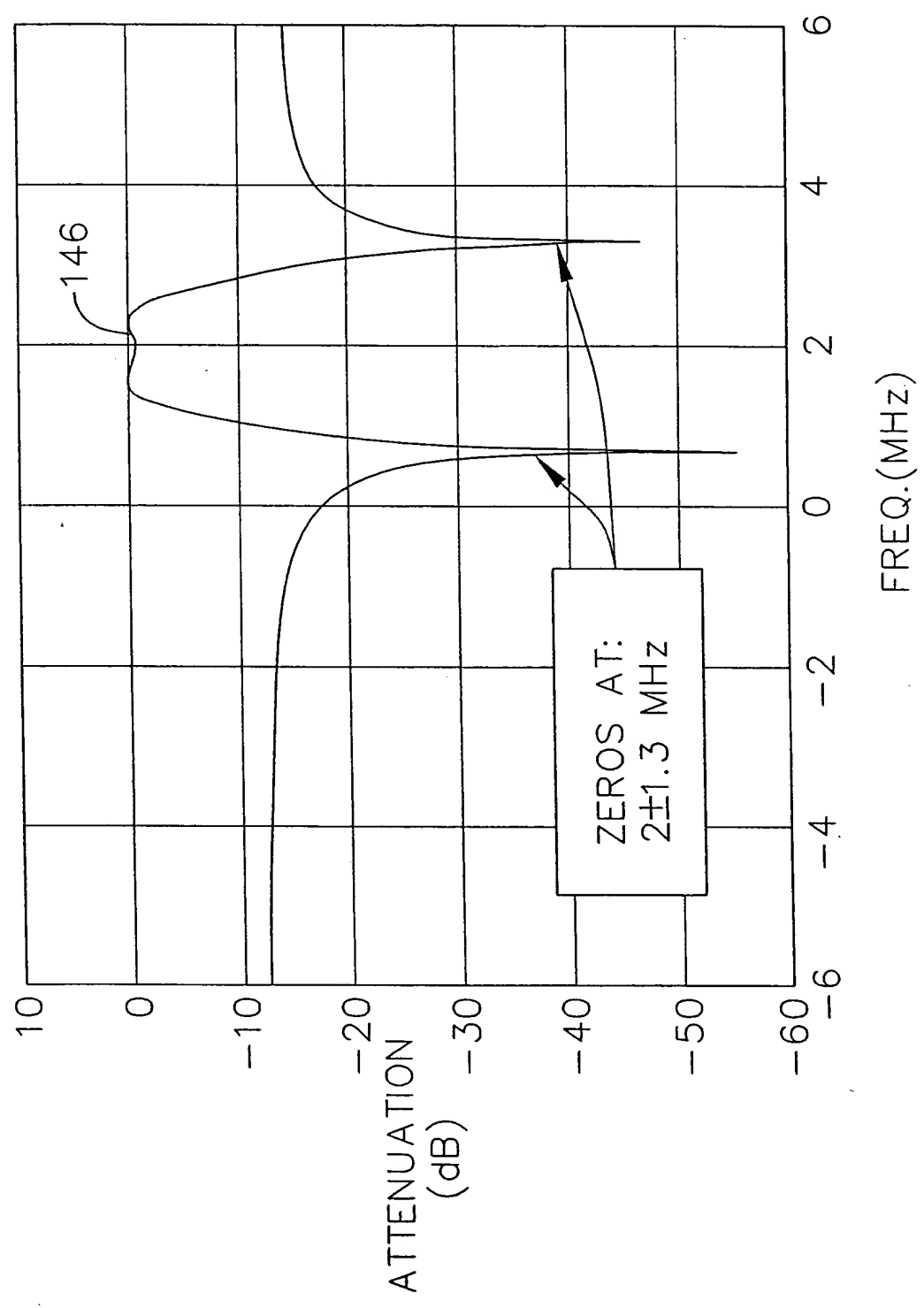




FIG. 12(a)

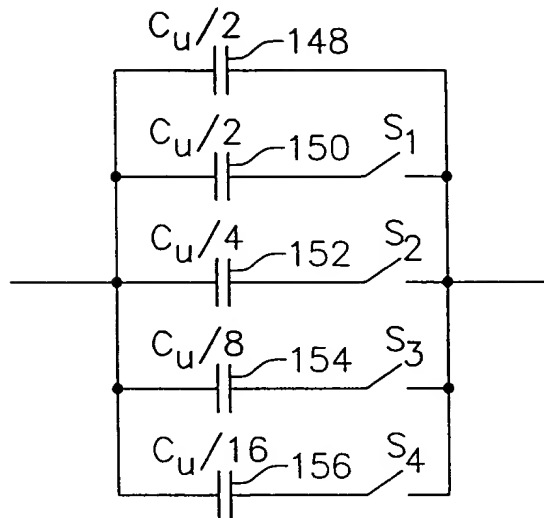


FIG. 12(b)

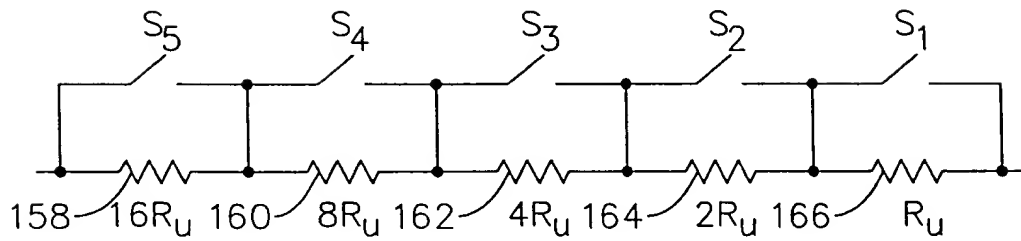


FIG. 13

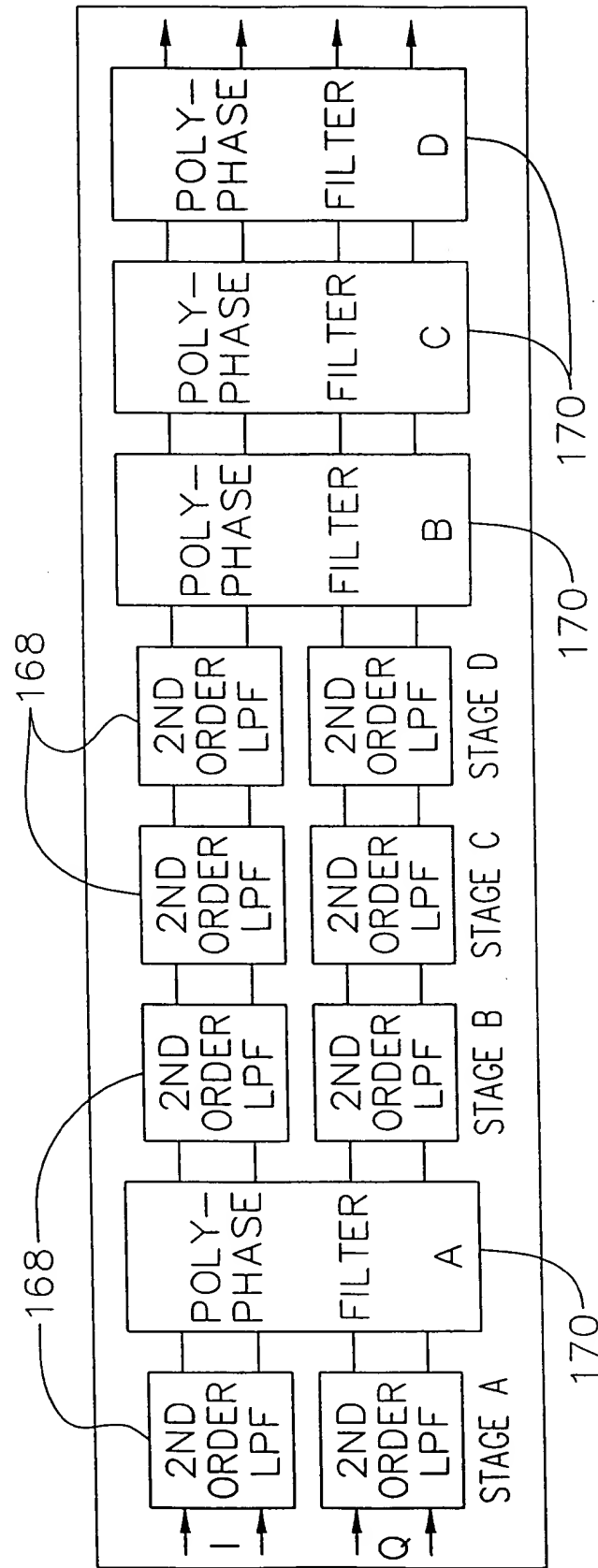




FIG. 14

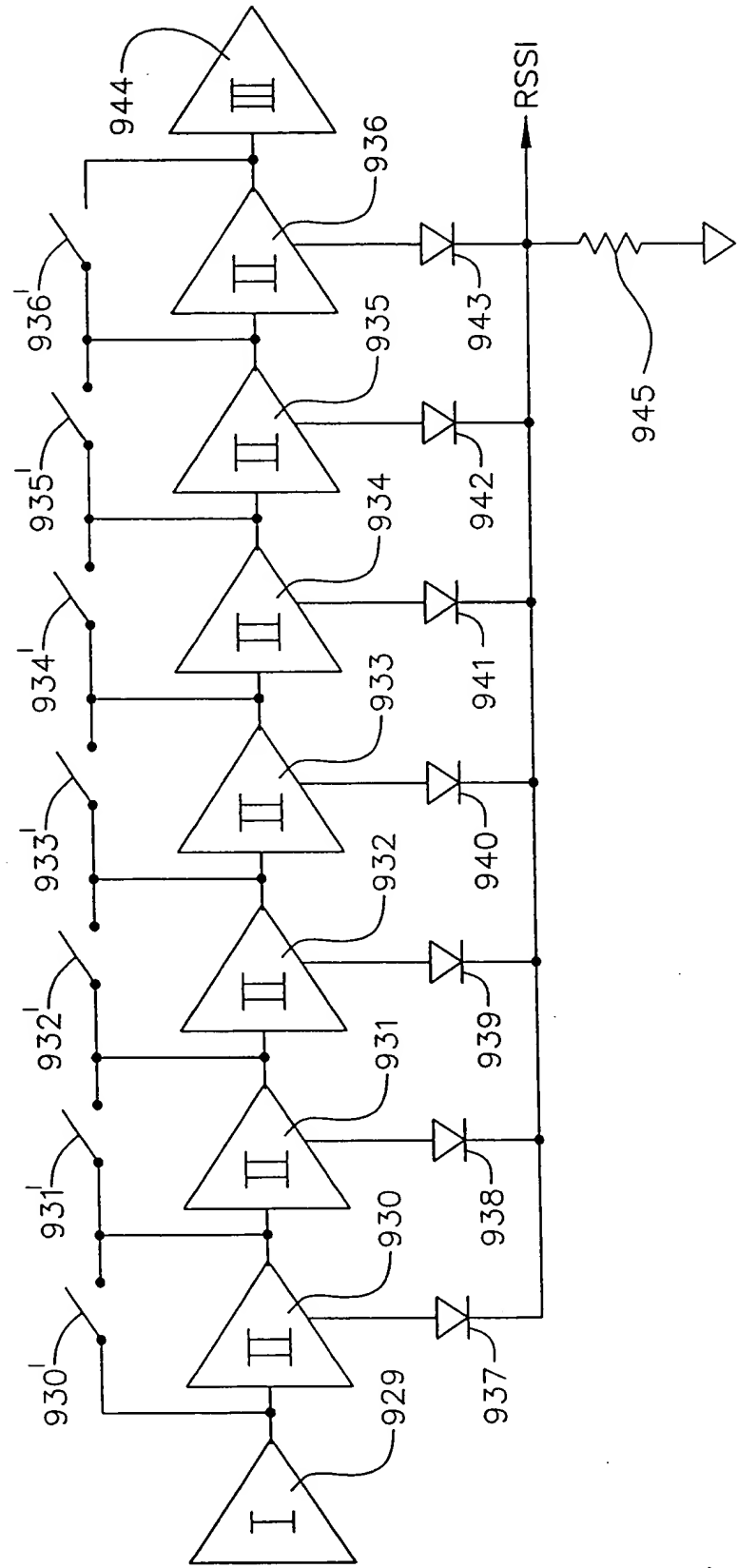




FIG. 15

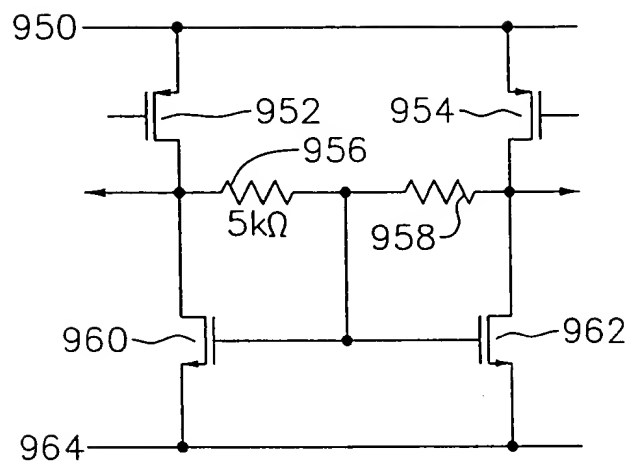


FIG. 16(a)

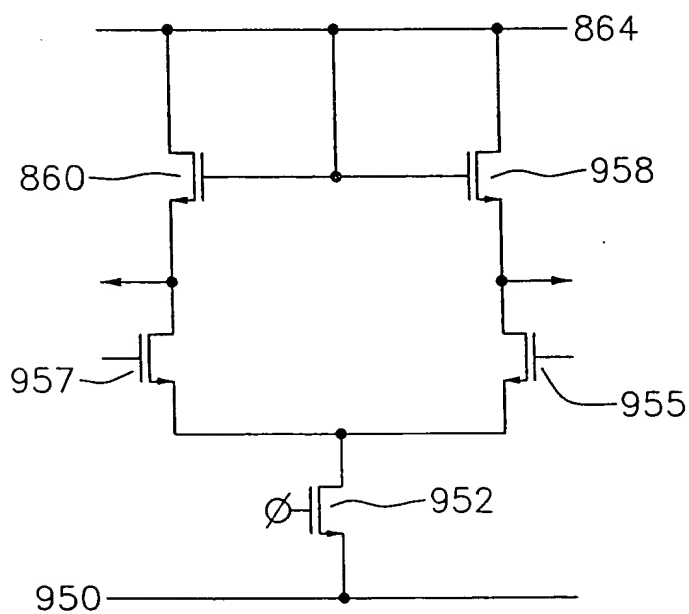
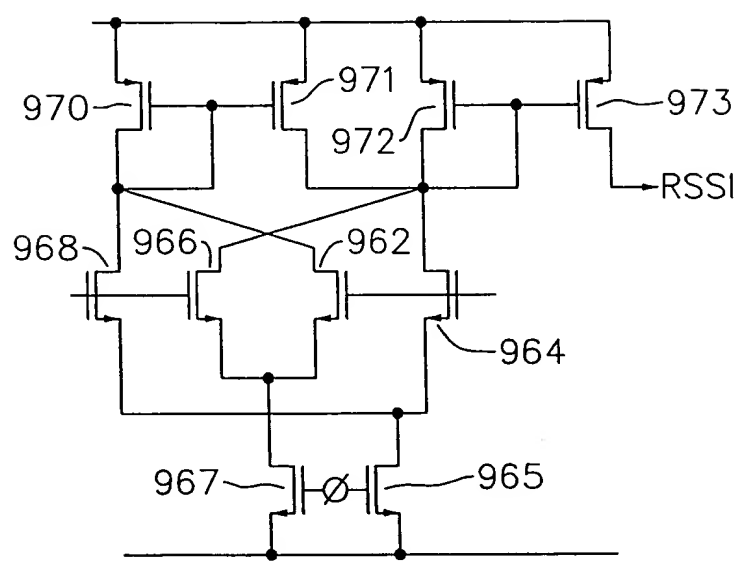




FIG. 16(b)



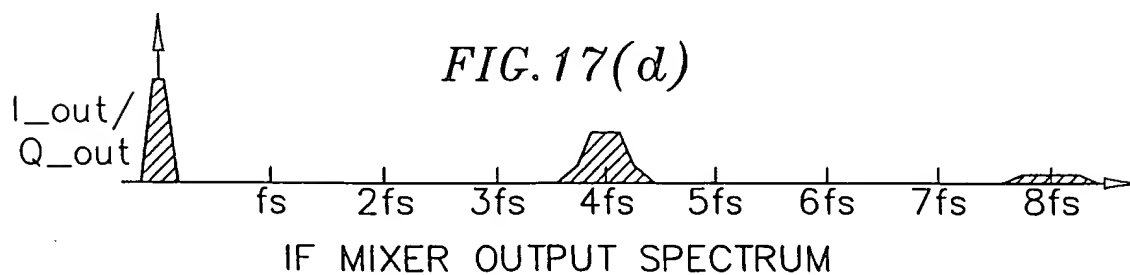
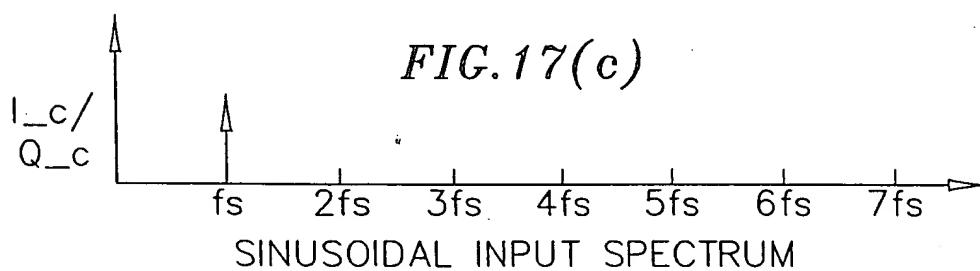
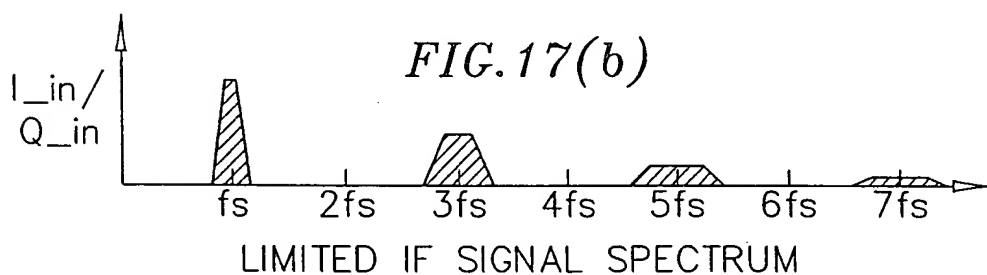
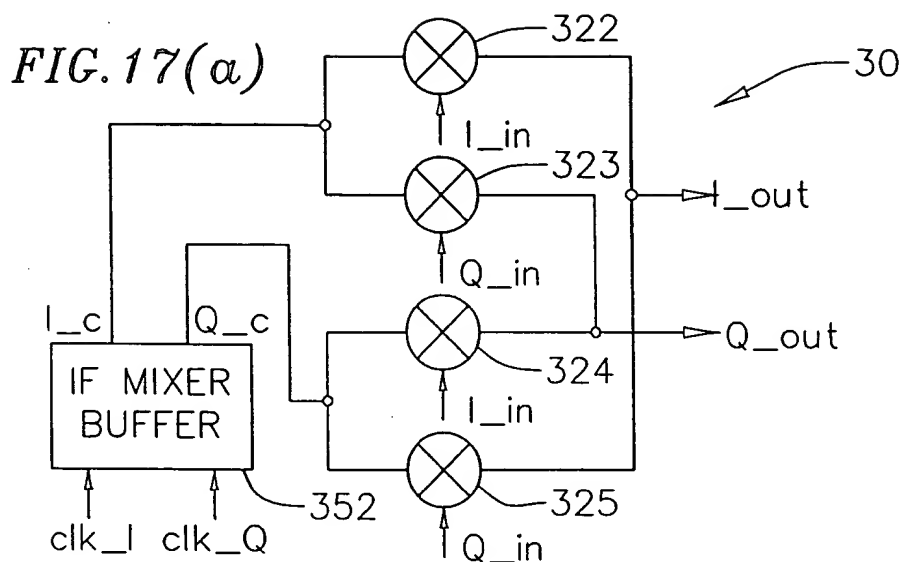


FIG. 18

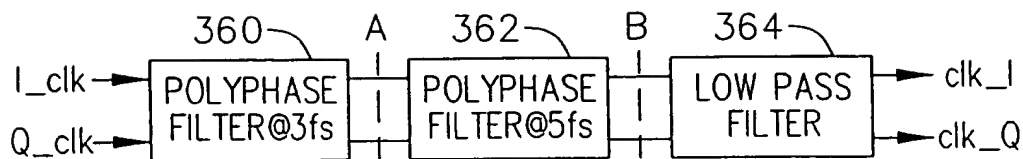


FIG. 19(a)

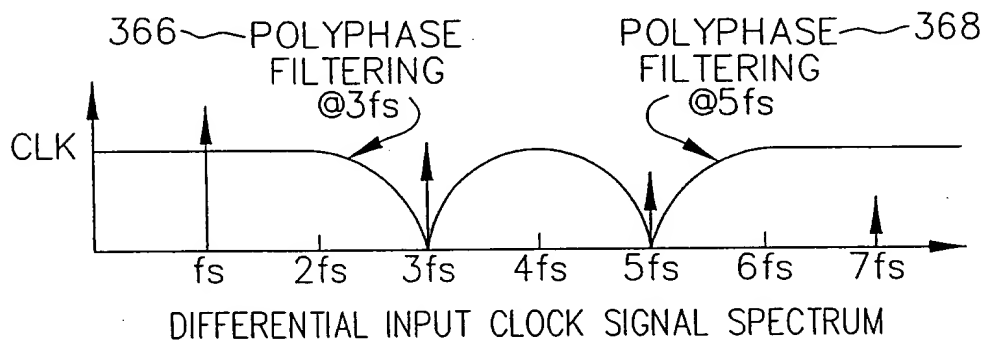


FIG. 19(b)

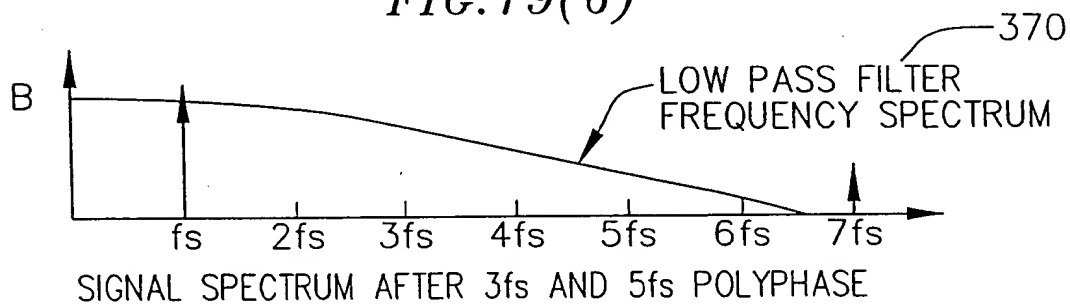


FIG. 19(c)

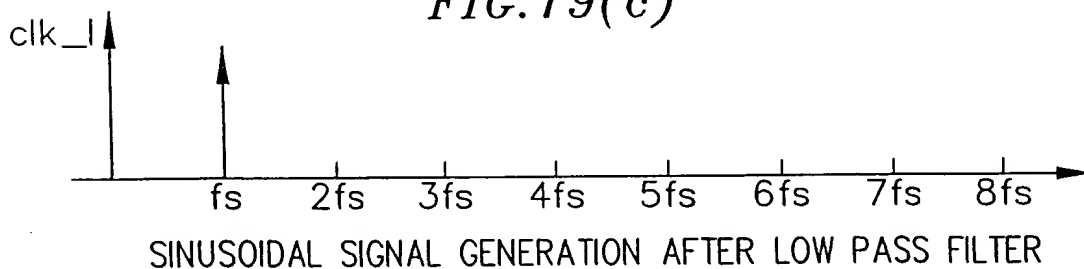




FIG.20(α)

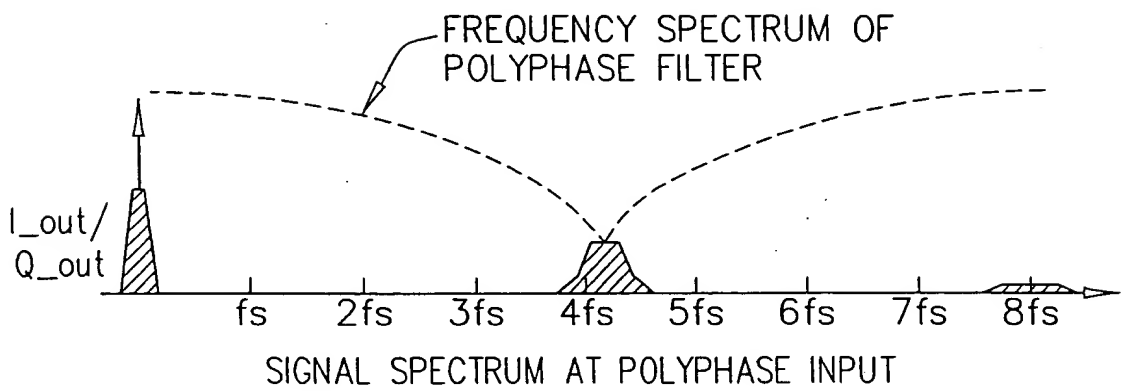


FIG.20(b)

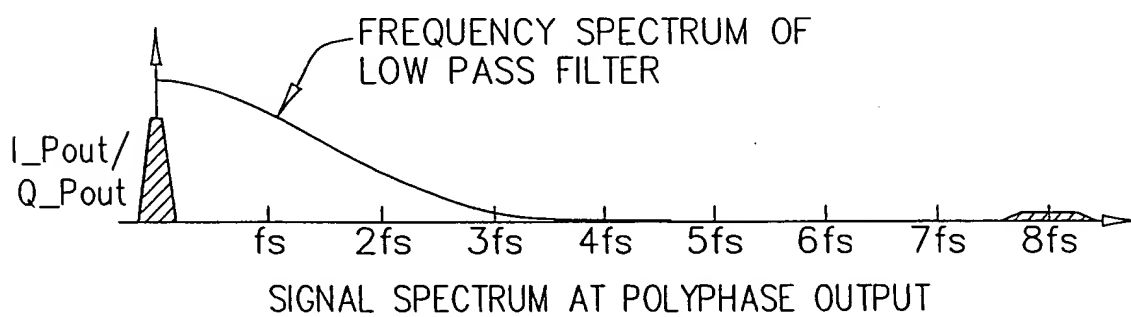


FIG.20(c)

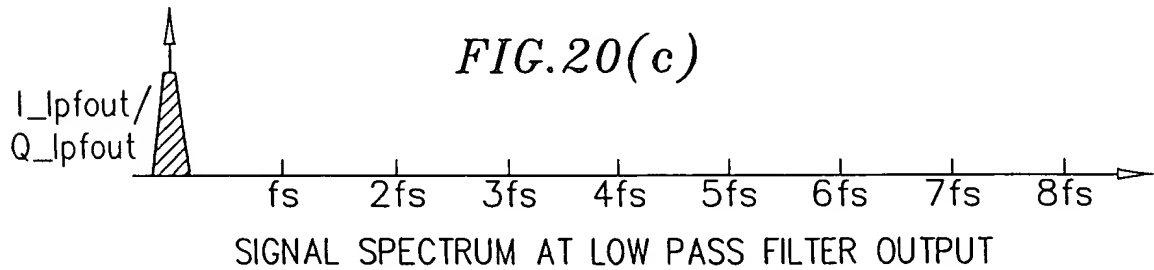


FIG.21

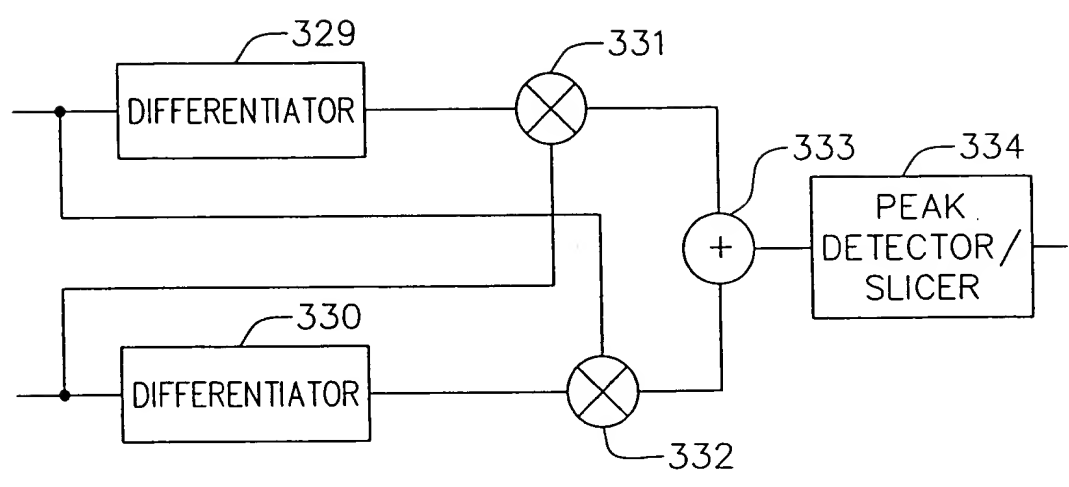
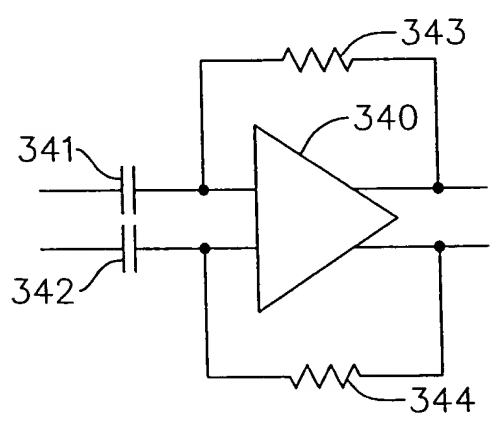


FIG.22



The diagram shows a differential signal processing circuit. Two input signals are fed into two comparators, 345 and 346. The output of comparator 345 is connected to a logic gate 350. The output of comparator 346 is connected to a logic gate 347. The outputs of logic gates 347 and 348 are connected to a logic gate 349. The output of logic gate 349 is connected to a logic gate 350. The circuit is labeled with reference numerals 345, 346, 347, 348, 349, and 350.

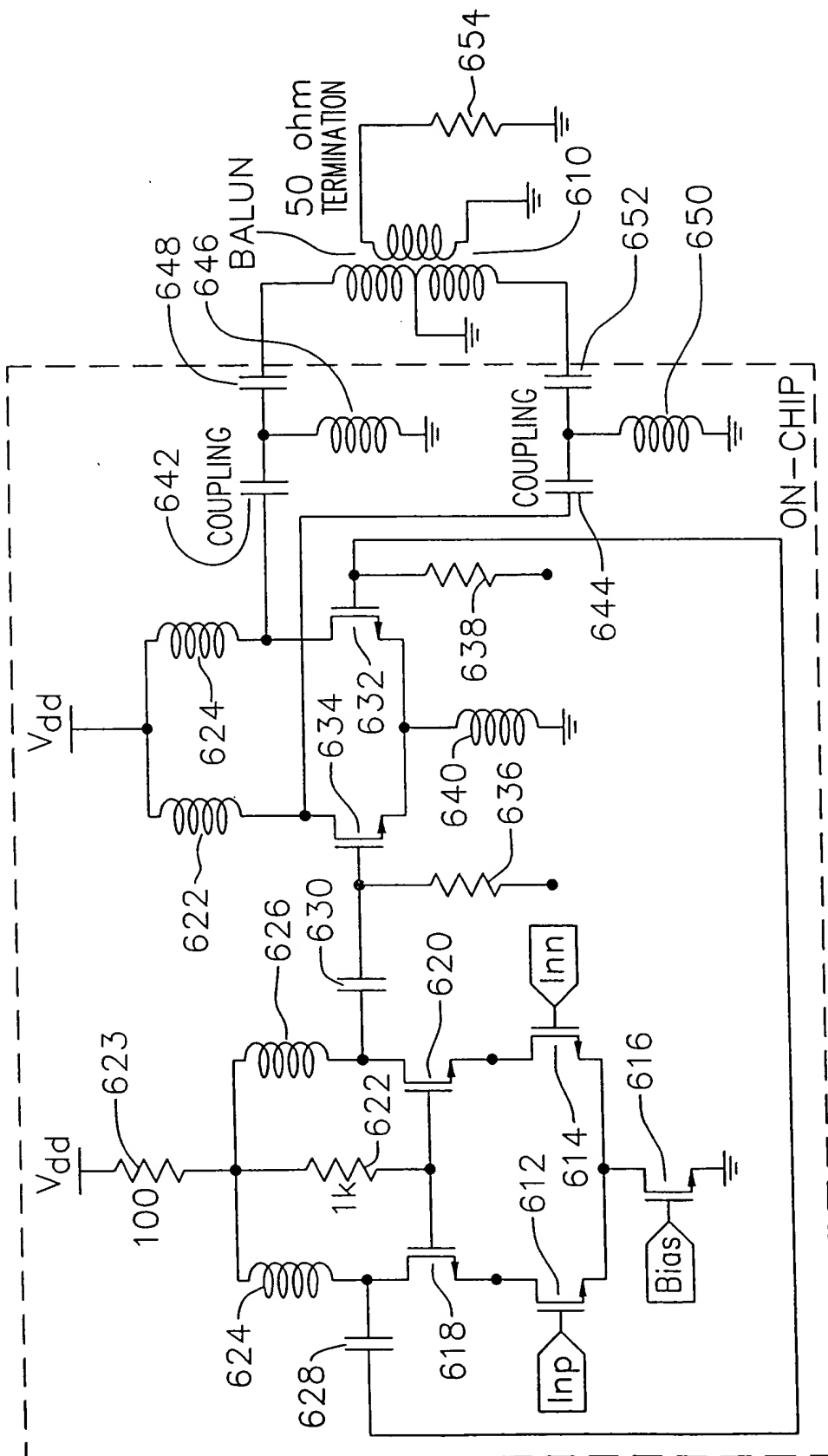


FIG.26(a)

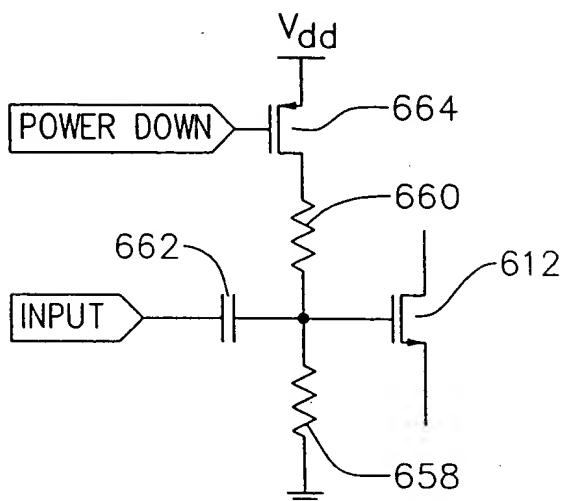


FIG.26(b)

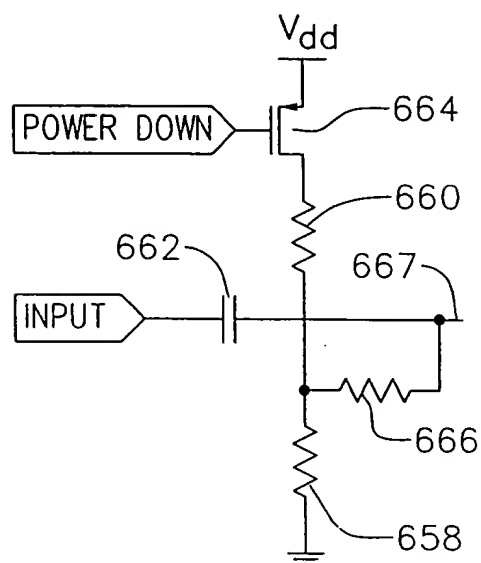


FIG.27

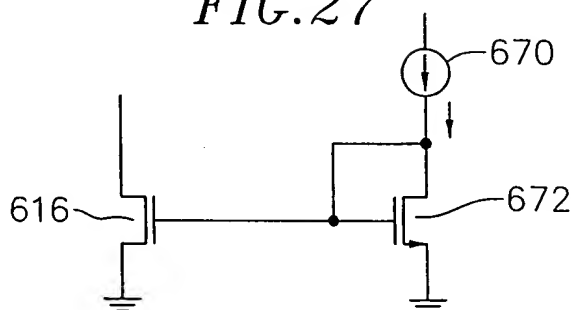


FIG.28

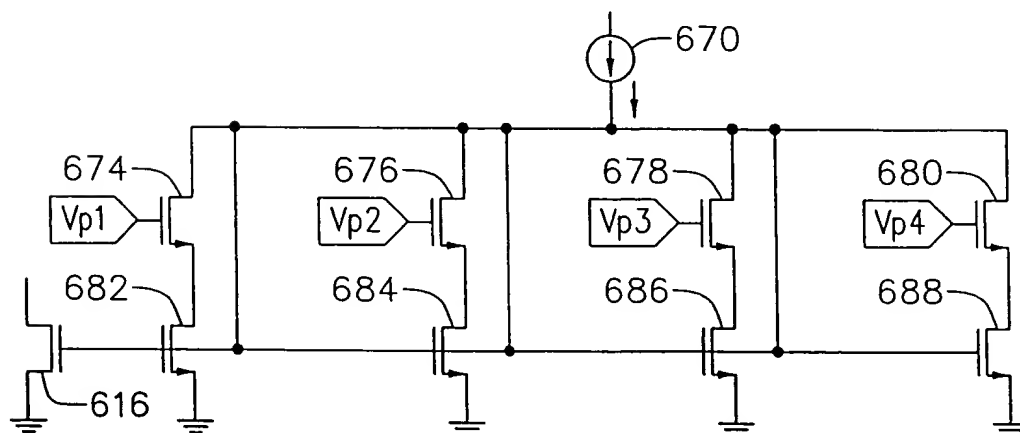


FIG. 29

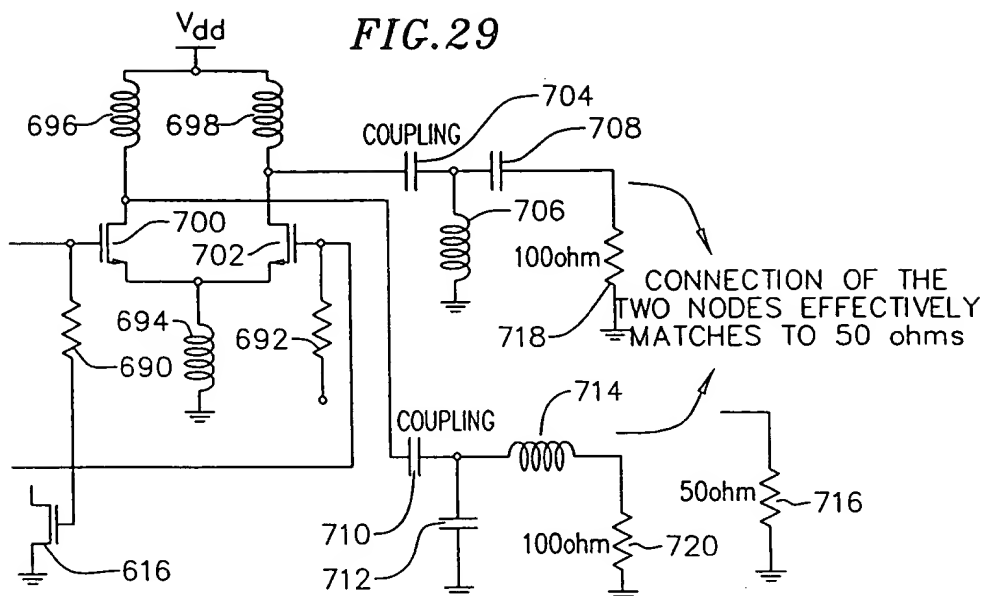


FIG. 30

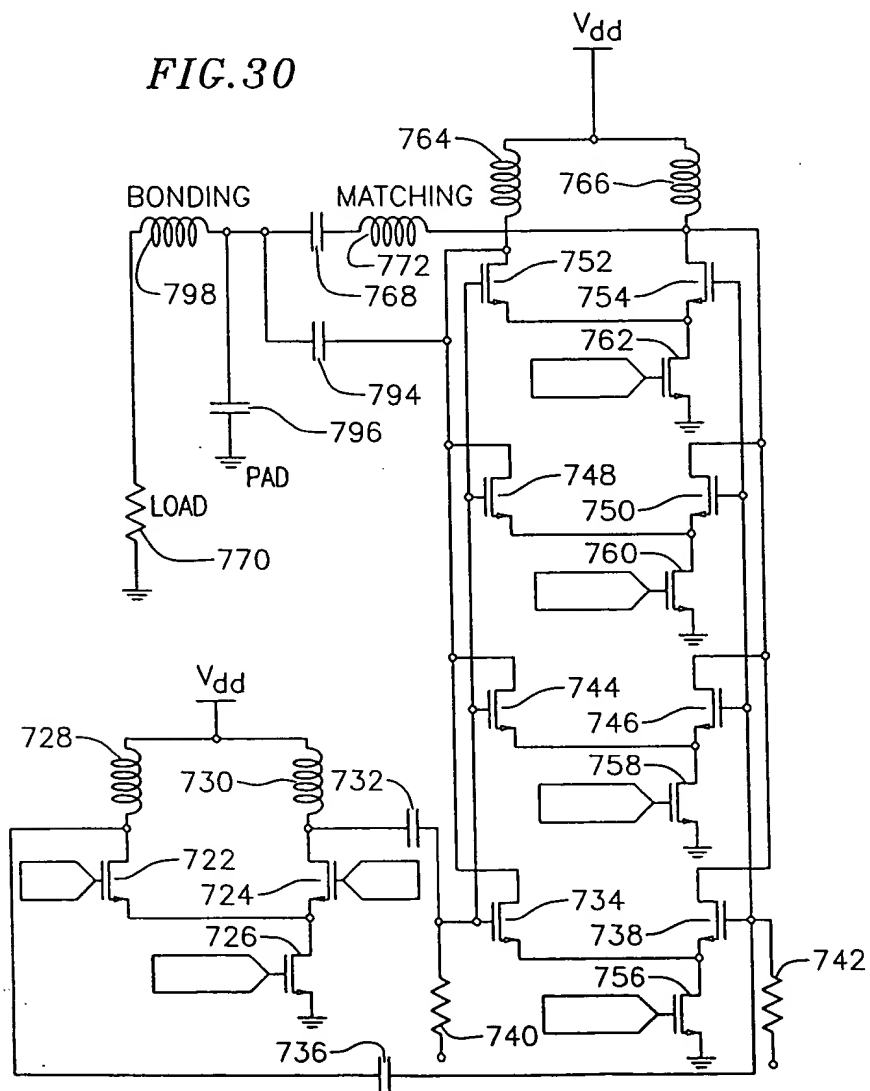


FIG. 31(a)

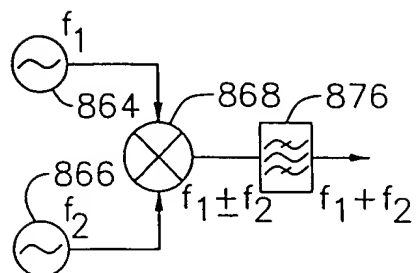


FIG. 31(b)

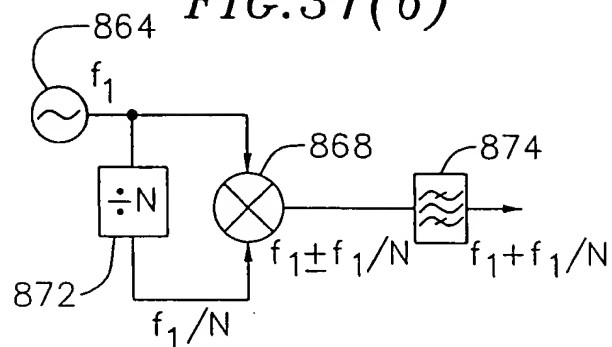


FIG. 32

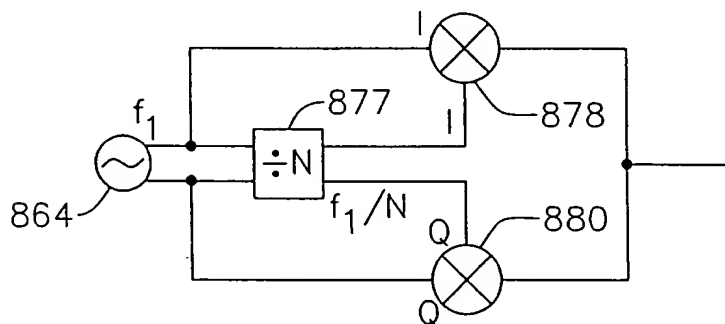


FIG. 33

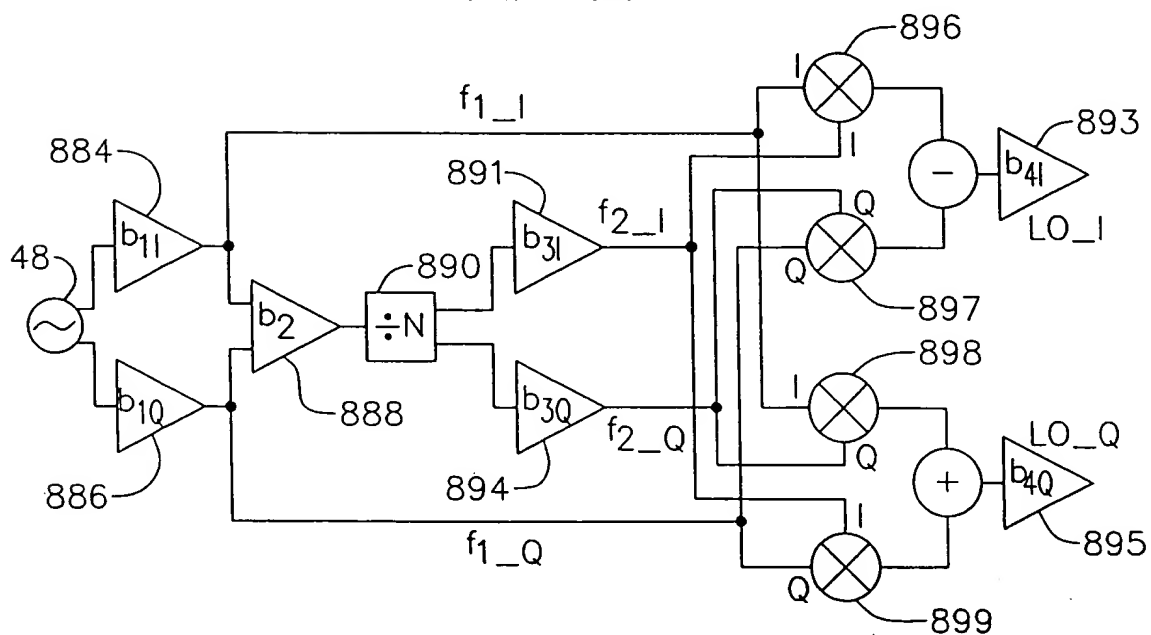


FIG.33(α)

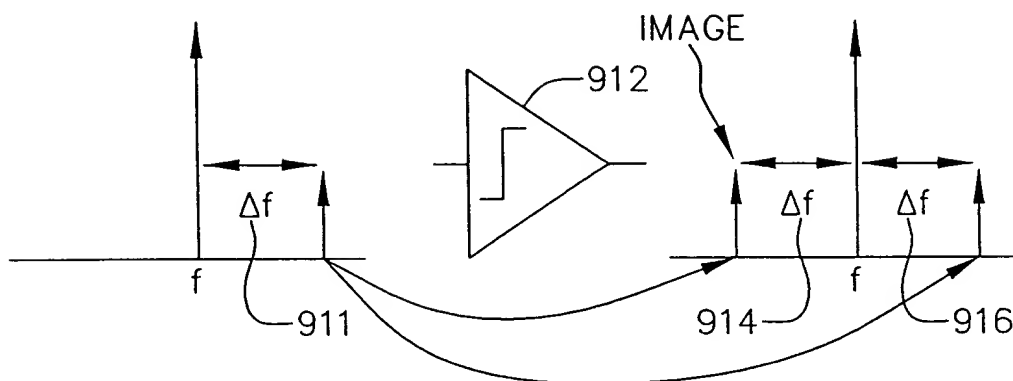


FIG.34

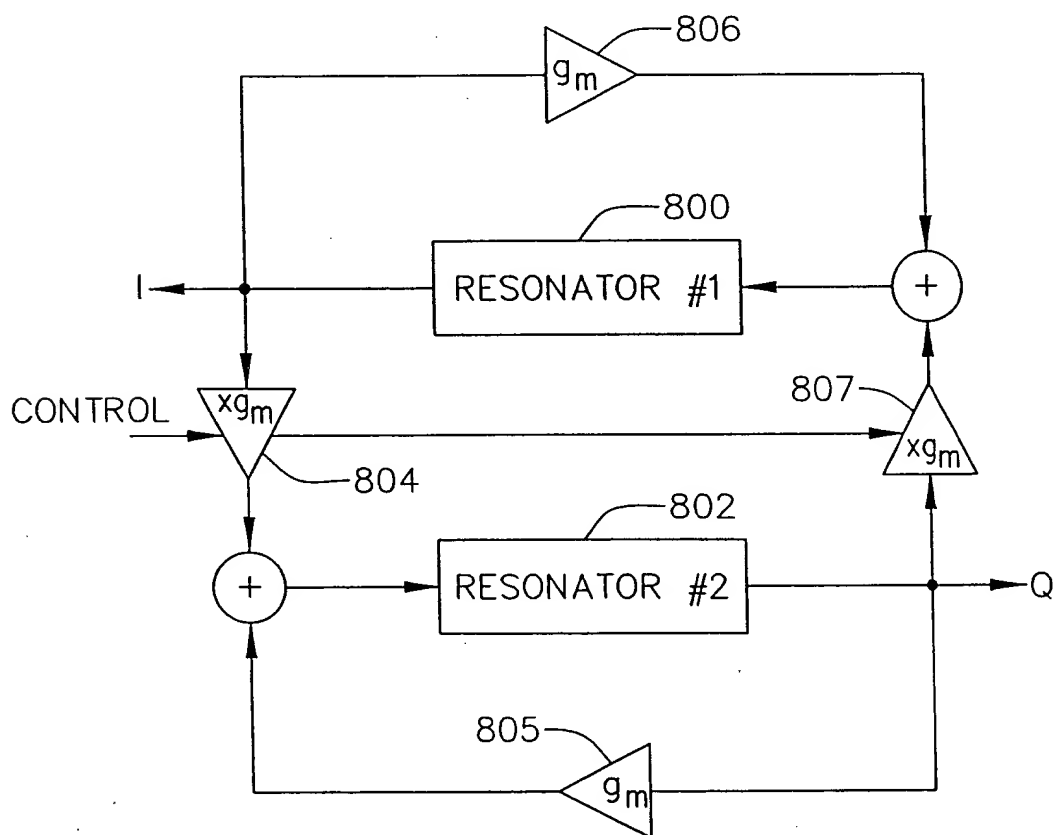
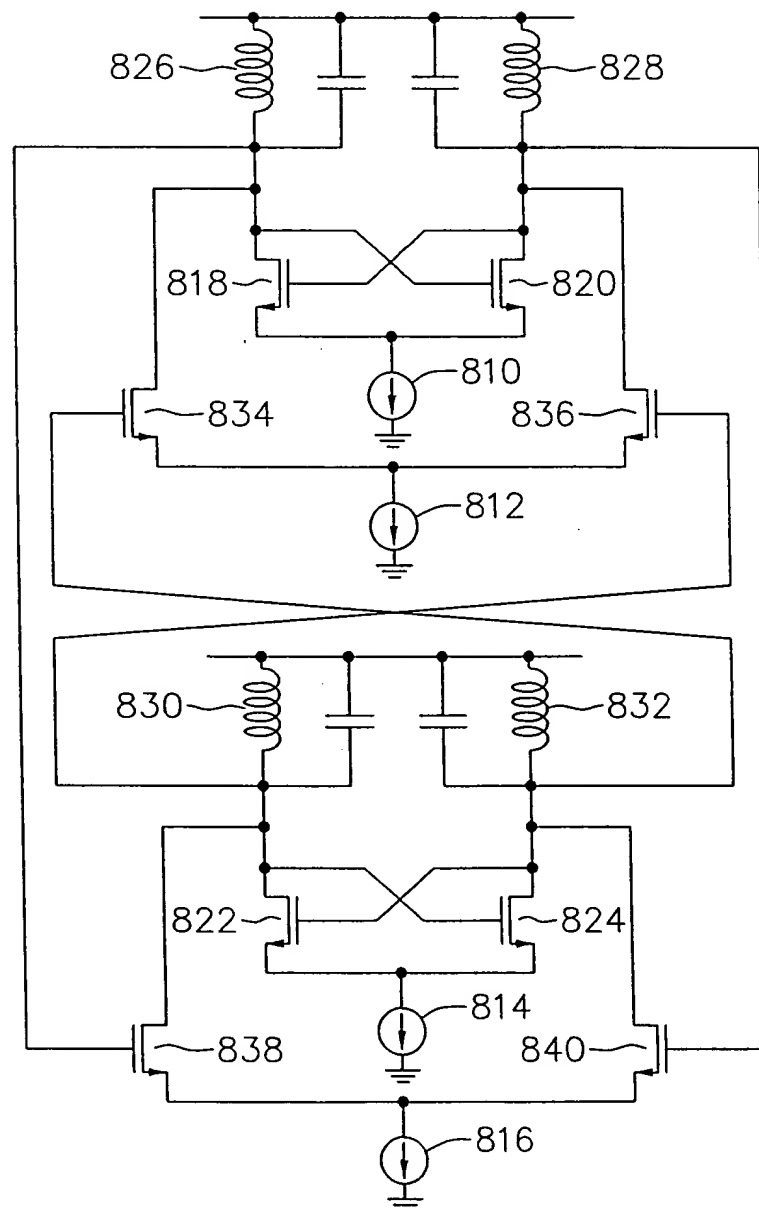


FIG. 35



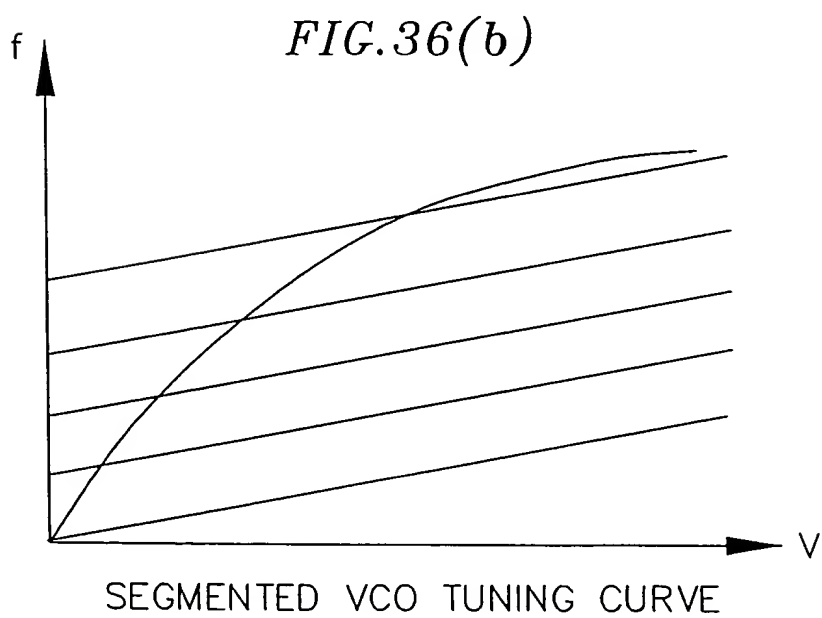
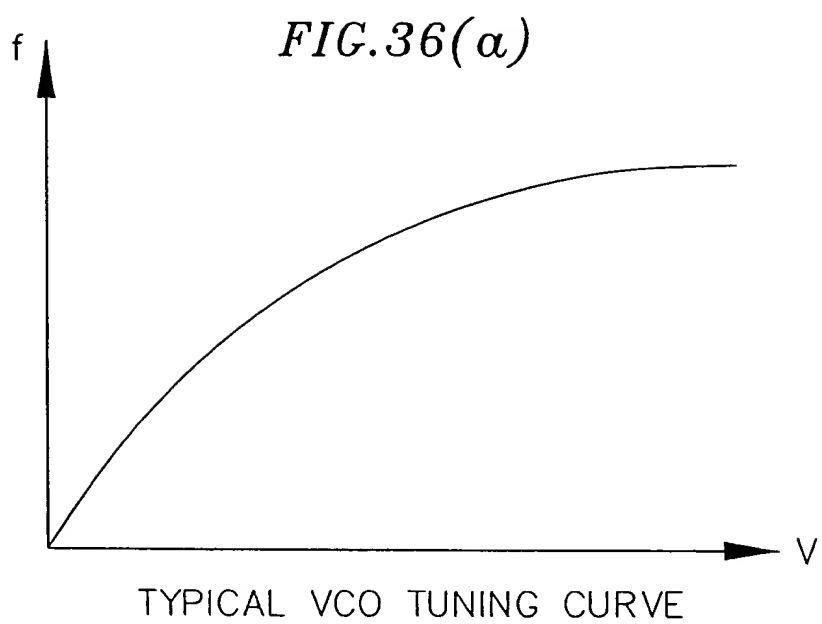




FIG.37(a)

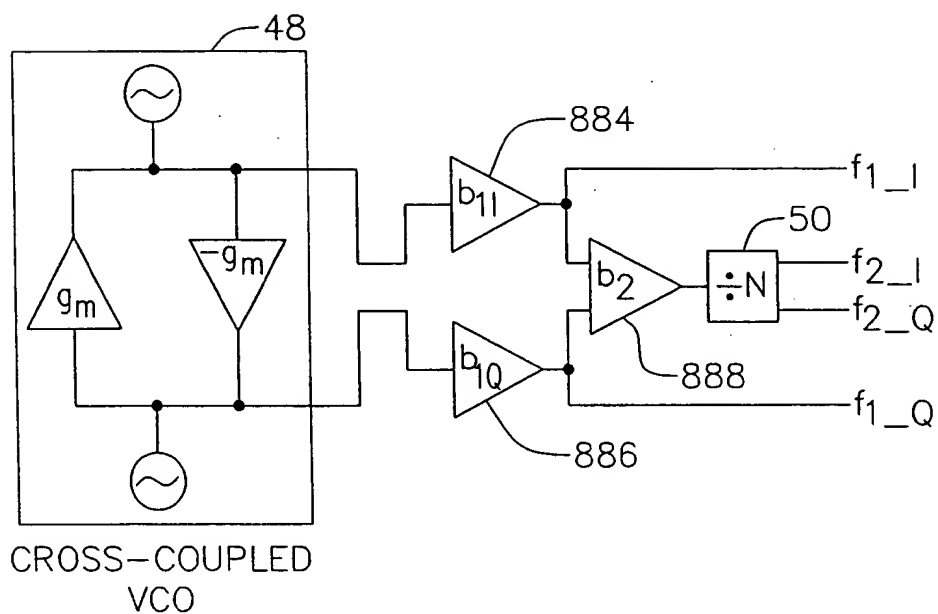


FIG.37(b)

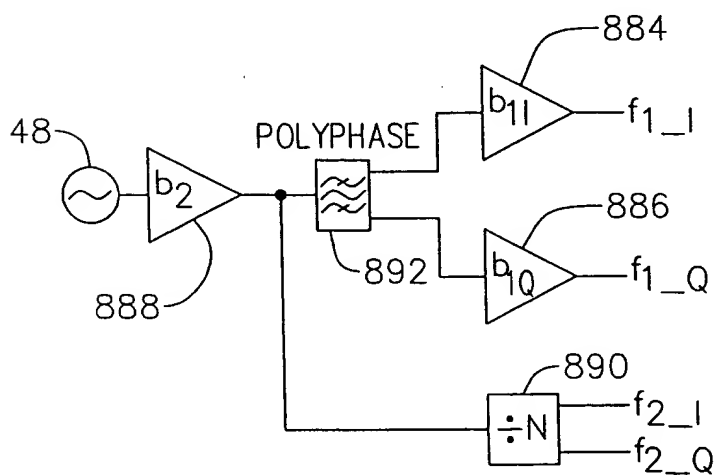
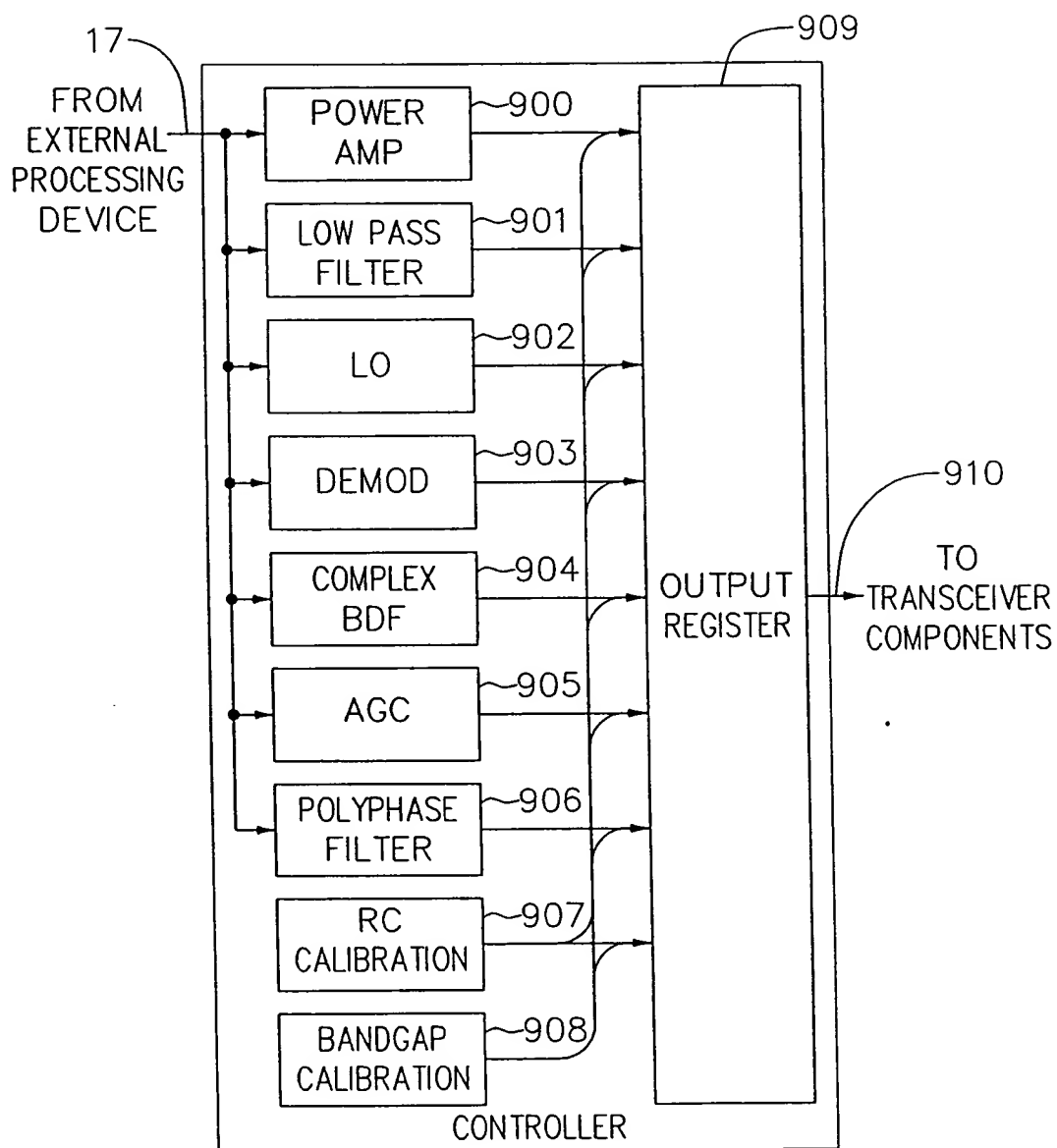




FIG. 38



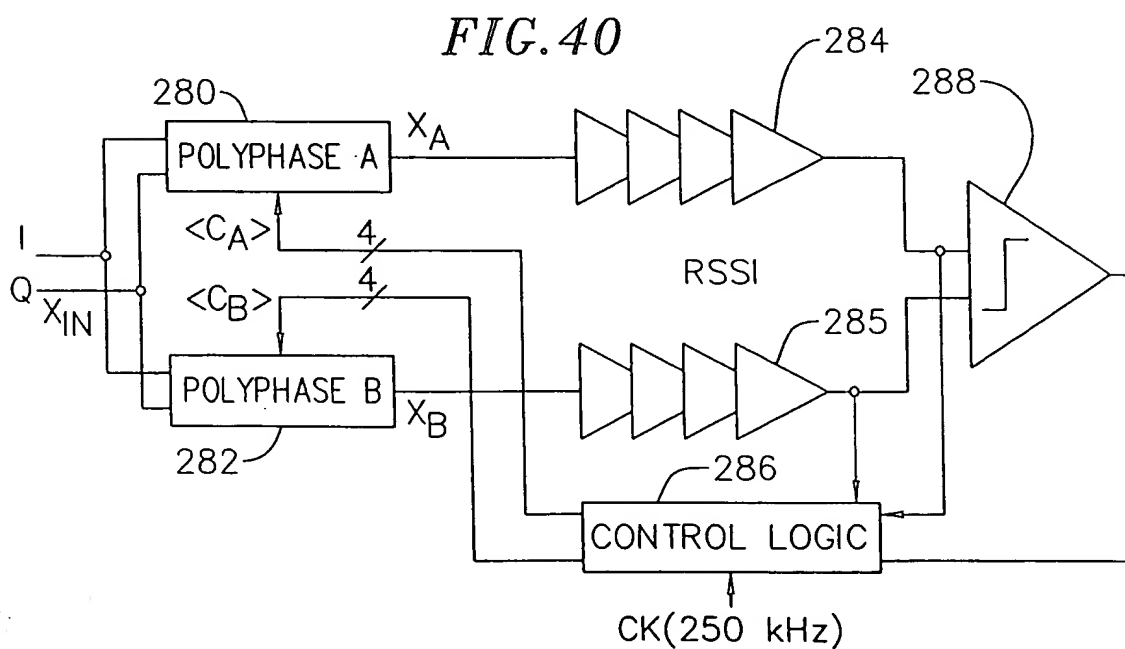
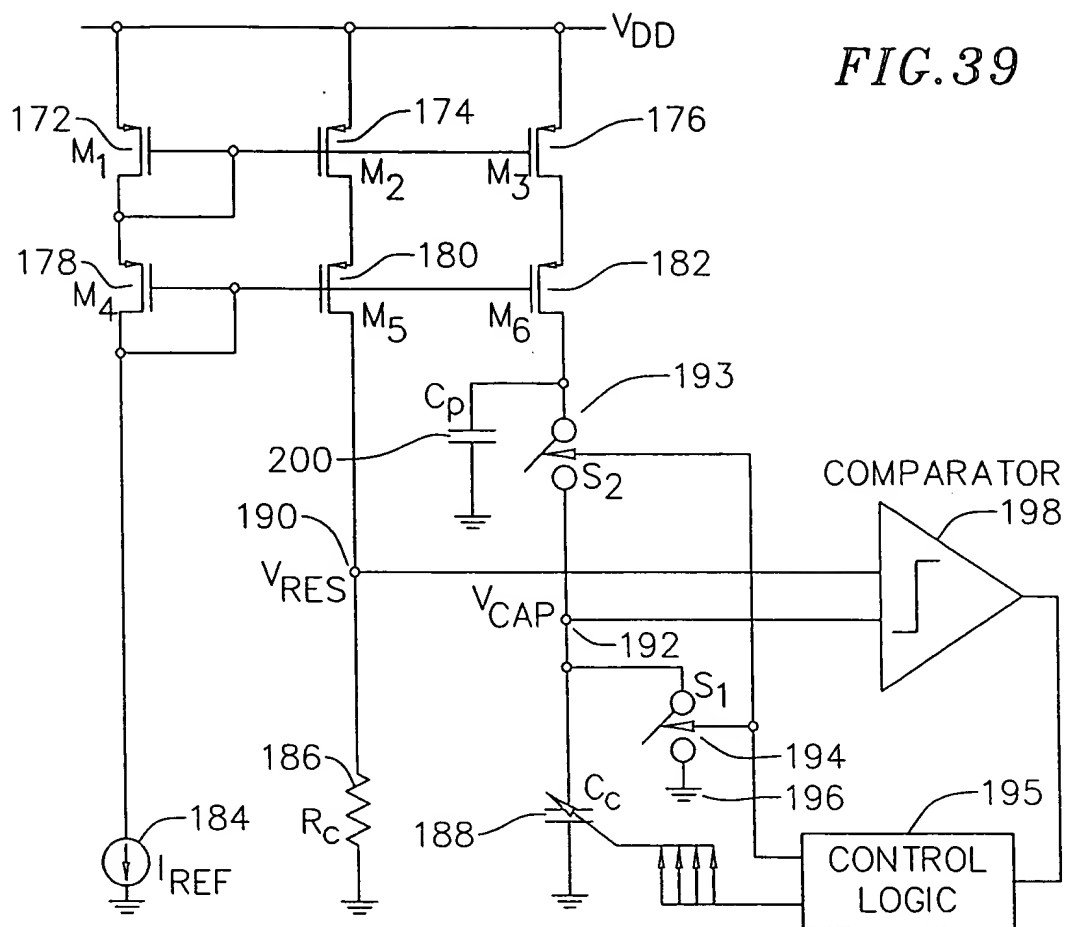


FIG. 41

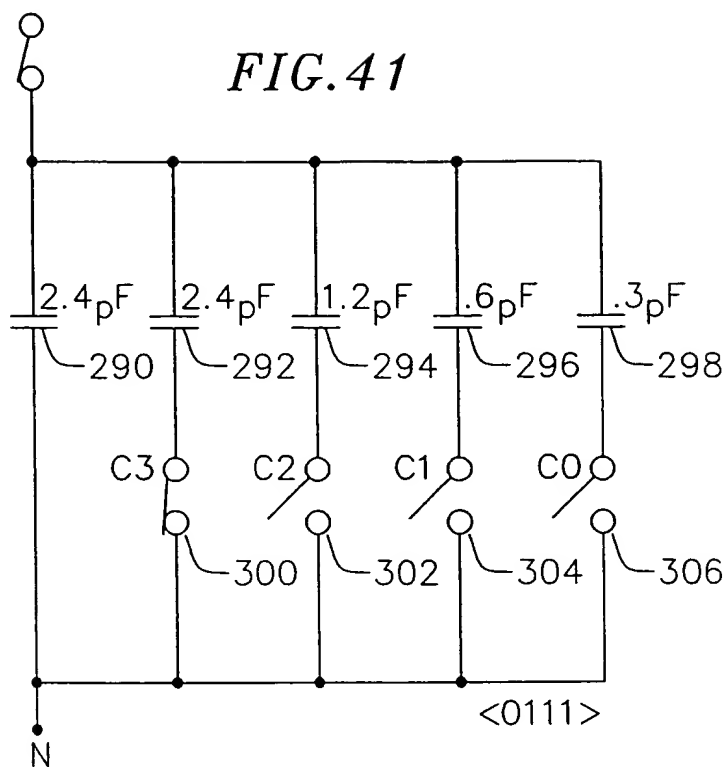


FIG. 42

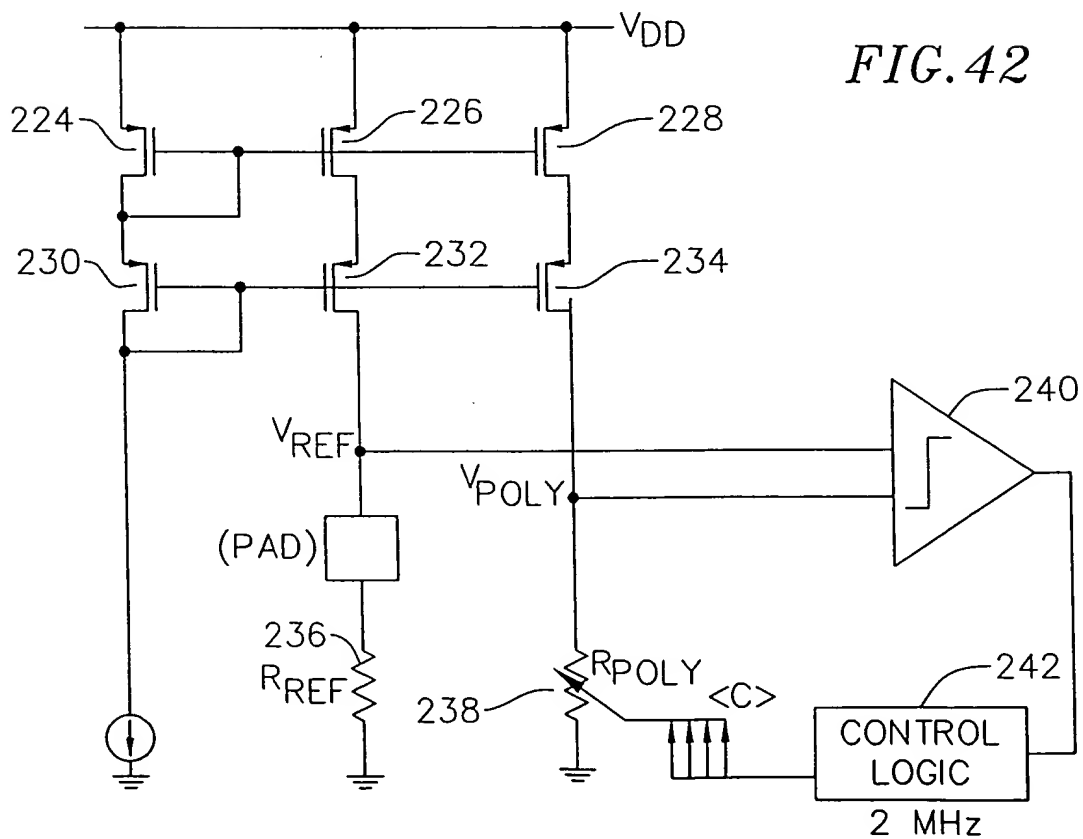


FIG. 46

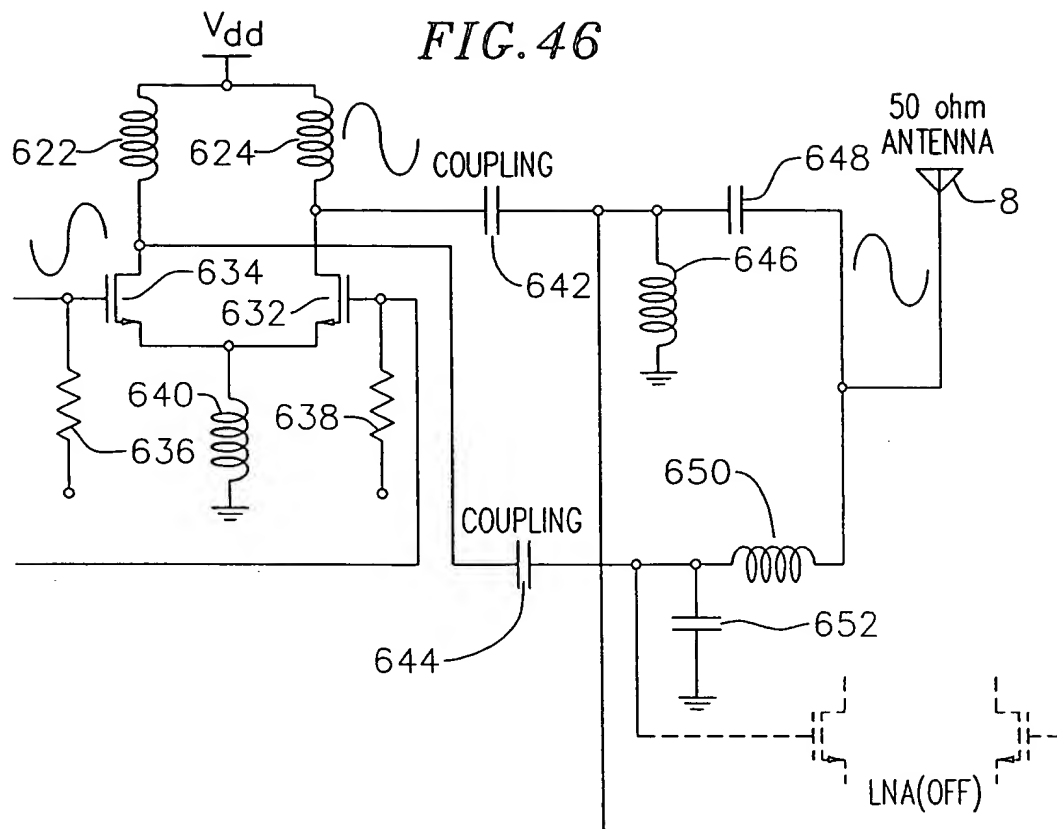


FIG. 47

